

PTO/SB/21 (09-04)

Approved for use through 07/31/2006. OMB 0651-0031

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission 456

| | |
|------------------------|-------------------|
| Application Number | 10/730,388 |
| Filing Date | December 07, 2003 |
| First Named Inventor | Buxton, et al. |
| Art Unit | 2863 |
| Examiner Name | Khuu, Cindy D. |
| Attorney Docket Number | TAI.0800 |

| ENCLOSURES (Check all that apply) | | |
|---|--|---|
| <input checked="" type="checkbox"/> Fee Transmittal Form <input checked="" type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input checked="" type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Reply to Missing Parts/ Incomplete Application <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53 | <input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation <input type="checkbox"/> Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____ <input type="checkbox"/> Landscape Table on CD | <input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): |
| <input type="text"/> Remarks Credit Card Payment Form, Form PTO/SS/08A, References (34 @ 441pp) | | |

| SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT | | | |
|--|------------------------|----------|--------|
| Firm Name | Noblitt & Gilmore, LLC | | |
| Signature | | | |
| Printed name | Daniel J. Noblitt | | |
| Date | 06 NOV 2006 | Reg. No. | 35,969 |

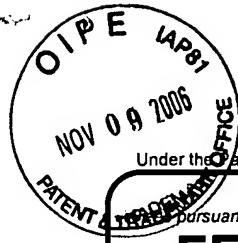
CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

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| Signature | | |
| Typed or printed name | Hannah E. Watts | Date 11/06/06 |

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PTO/SB/17 (07-06)

Approved for use through 01/31/2007. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.

Section 804(d) of the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL For FY 2006

Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$)
180.00

Complete if Known

| | |
|----------------------|-------------------|
| Application Number | 10/730,388 |
| Filing Date | December 07, 2003 |
| First Named Inventor | Buxton, et al. |
| Examiner Name | Khuu, Cindy D. |
| Art Unit | 2863 |
| Attorney Docket No. | TAI.0800 |

METHOD OF PAYMENT (check all that apply)

Check Credit Card Money Order None Other (please identify): _____

Deposit Account Deposit Account Number: 50-2993 Deposit Account Name: Noblitt & Gilmore, LLC

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

Charge fee(s) indicated below Charge fee(s) indicated below, except for the filing fee
 Charge any additional fee(s) or underpayments of fee(s) Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

| Application Type | FILING FEES | | SEARCH FEES | | EXAMINATION FEES | | <u>Fees Paid (\$)</u> |
|------------------|-----------------|---------------------|-----------------|---------------------|------------------|---------------------|-----------------------|
| | <u>Fee (\$)</u> | <u>Small Entity</u> | <u>Fee (\$)</u> | <u>Small Entity</u> | <u>Fee (\$)</u> | <u>Small Entity</u> | |
| Utility | 300 | 150 | 500 | 250 | 200 | 100 | _____ |
| Design | 200 | 100 | 100 | 50 | 130 | 65 | _____ |
| Plant | 200 | 100 | 300 | 150 | 160 | 80 | _____ |
| Reissue | 300 | 150 | 500 | 250 | 600 | 300 | _____ |
| Provisional | 200 | 100 | 0 | 0 | 0 | 0 | _____ |

2. EXCESS CLAIM FEES

Fee Description

Each claim over 20 (including Reissues)

Small Entity

Fee (\$) Fee (\$)

50 25

Each independent claim over 3 (including Reissues)

200 100

Multiple dependent claims

360 180

Total Claims

Extra Claims

Fee (\$)

Fee Paid (\$)

Multiple Dependent Claims

Fee (\$) Fee Paid (\$)

- 20 or HP = _____ x _____ = _____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims

Extra Claims

Fee (\$)

Fee Paid (\$)

Fee (\$) Fee Paid (\$)

- 3 or HP = _____ x _____ = _____

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

| | | | | |
|---------------------|---------------------|---|-----------------|----------------------|
| <u>Total Sheets</u> | <u>Extra Sheets</u> | <u>Number of each additional 50 or fraction thereof</u> | <u>Fee (\$)</u> | <u>Fee Paid (\$)</u> |
|---------------------|---------------------|---|-----------------|----------------------|

_____ - 100 = _____ / 50 = _____ (round up to a whole number) x _____ = _____

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Fees Paid (\$)

Other (e.g., late filing surcharge): Information Disclosure Statement

180.00

SUBMITTED BY

Signature

Registration No.
(Attorney/Agent) 35,969

Telephone 480-994-9859

Name (Print/Type) Daniel J. Noblitt

Date 05 Nov 2006

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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PATENT

IN THE UNITED STATES PATENT AND
TRADEMARK OFFICE

Inventor: Buxton, et al.

Docket No.: TAI.0800

Serial No.: 10/730,388

Examiner: Khuu, Cindy D.

Filing Date: December 07, 2003

Art Unit: 2863

Title: Methods and Apparatus for Data
Analysis

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner of Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Commissioner:

In accordance with the duty of disclosure under 37 C.F.R. §1.56 and pursuant to 37 C.F.R. §§1.97-1.98, the reference or references listed and identified on the attached PTO/SB/08-based form are being submitted for consideration by the Examiner.

The applicant further provides the following information for which no written references are possessed:

- KLA-Tencor may have products known as Integrator or Navigator in the field of testing that may be relevant;
- The company Electroglas may have products in the field of testing that may be relevant;
- The company Knights Technology may have a product called "Star" that may be relevant;
- A Korean company or product known as "Defector 2" may be relevant;

- A company known as IDS may have products in the field of testing that may be relevant;
- Motorola may have products in the field of testing that may be relevant;
- Syntricity Alcatel may have products in the field of testing that may be relevant;
- ST Microelectronics may have products in the field of testing that may be relevant;
- Pintail may have products in the field of testing that may be relevant;
- Galaxy may have products in the field of testing that may be relevant;
- A company known as I2 may have products in the field of testing that may be relevant;
- Freescale may have products in the field of testing that may be relevant;
- Yield Dynamics may have products in the field of testing that may be relevant;
- Brooks/PRI Automation may have products in the field of testing that may be relevant; and
- Enclosed is a bibliography of potentially relevant references. At this time the referenced documents are unavailable.

The preceding information and the attached references are cited only in the interest of candor and without any admission that they constitute statutory prior art or contain matter which anticipates the invention or which would render the same obvious, either singly or in combination, to a person of ordinary skill in the art.

Inventor: Buxton, et al.
Serial No.: 10/730,388
Filed: December 07, 2003

This Information Disclosure Statement (IDS) is being filed under 37 C.F.R. §1.97(c) before the mailing date of any final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311, or an action that otherwise closes prosecution of the application. The IDS is accompanied by the fee set forth in 37 C.F.R. §1.17(p). If there are any questions concerning this IDS, the Examiner is requested to contact the undersigned.

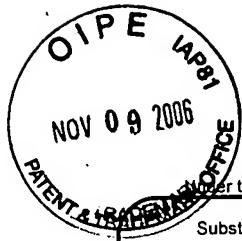
Respectfully submitted,

Date: 06 NOV 2006

By: 

Daniel J. Noblitt
Reg. No. 35,969

NOBLITT & GILMORE, LLC
4800 North Scottsdale Road
Suite 6000
Scottsdale, Arizona 85251
Telephone: 480.994.9859
Facsimile: 480.994.9025



PTO/SB/08A (07-05)

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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 5

| Complete if Known | |
|--------------------------|-------------------|
| Application Number | 10/730,388 |
| Filing Date | December 07, 2003 |
| First Named Inventor | Buxton, et al. |
| Art Unit | 2863 |
| Examiner Name | Khuu, Cindy D. |
| Attorney Docket Number | TAI.0800 |

U. S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

| | | | |
|-----------------------|--|--------------------|--|
| Examiner Signature | | Date Considered | |
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| <p>Substitute for form 1449/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p>(Use as many sheets as necessary)</p> | | <i>Complete if Known</i> | |
| | | Application Number | 10/730,388 |
| | | Filing Date | December 07, 2003 |
| | | First Named Inventor | Buxton, et al. |
| | | Art Unit | 2863 |
| | | Examiner Name | Khuu, Cindy D. |
| Sheet 2 of 5 | Attorney Docket Number | TAI.0800 | |

| NON PATENT LITERATURE DOCUMENTS | | | |
|---------------------------------|-----------------------|---|----------------|
| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
| | | SINGH Et al., Screening for Known Good Die (KGD) Based on Defect Clustering: An Experimental Study, IEEE | |
| | | SINGH, Position Statement: Good Die in Bad Neighborhoods, IEEE | |
| | | MILLER, Position Statement: Good Die in Bad Neighborhoods, IEEE | |
| | | ROEHR, Position Statement: Good Die in Bad Neighborhoods, IEEE | |
| | | MANN, "Leading Edge" of Wafer Level Testing | |
| | | MICHELSON, Statistically Calculating Reject Limits at Parametric Test, IEEE | |
| | | SABADE et al., Immediate Neighbor Difference IDDQ Test (INDIT) for Outlier Detection, Dept. of Computer Science – Texas A&M University | |
| | | HUANG, et al., Image Processing Techniques for Wafer Defect Cluster Identification, IEEE | |
| | | SABADE, et al., Use of Multiple IDDQ Test Metrics for Outlier Identification, Dept. of Computer Science – Texas A&M University | |
| | | CHEN, et al., A Neural-Network Approach to Recognize Defect Spatial Pattern in Semiconductor Fabrication, IEEE | |

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| | | First Named Inventor | Buxton, et al. |
| | | Art Unit | 2863 |
| (Use as many sheets as necessary) | | Examiner Name | Khuu, Cindy D. |
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| | | Attorney Docket Number | TAI.0800 |

| NON PATENT LITERATURE DOCUMENTS | | | |
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| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
| | | SAPOZHNIKOVA, et al., The Use of dARTMAP and FUZZY ARTMAP to Solve the Quality Testing Task in Semiconductor Industry, IEEE | |
| | | SIKKA, Automated Feature Detection & Characterization in Sort Wafer Maps, | |
| | | HANSEN, et al., Process Improvement Through the Analysis of Spatially Clustered Defects on Wafer Maps | |
| | | DENBY, et al., A Graphical User Interface for Spatial Data Analysis in Integrated Circuit Manufacturing, AT&T Bell Laboratories | |
| | | FRIEDMAN, et al., Model-Free Estimation of Defect Clustering in Integrated Circuit Fabrication | |
| | | HANSEN, et al., Monitoring Wafer Map Data From Integrated Circuit Fabrication Processes for Spatially Clustered Defects | |
| | | XU, Statistical Problems in Semiconductor Manufacturing | |
| | | THOMAS GNIETING, Measurement Related and Model Parameter Related Statistics | |
| | | Agilent PDQ-WLR(tm) Test and Analysis Software Environment - Product Note, Agilent Technologies, 2000 | |
| | | Advance Parametric Tester with HP SPECS, Hewlett-Packard Company, 1999 | |

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| Examiner Signature | | Date Considered | |
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| | | | | Examiner Name | Khuu, Cindy D. |
| Sheet | 4 | of | 5 | Attorney Docket Number | TAI.0800 |

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| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | | | | T ² |
| | | JEFF CHAPPELL, LSI Applies Statistics to Defectivity, 4/14/2003 (http://www.reed-electronics.com/electronicnews/index.asp?layout=articlePrint&articleID=CA292185) | | | | |
| | | ERIK JAN MARINISSEN, et al., Creating Value Through Test, IEEE 2003, 1530-1591 | | | | |
| | | RUSSELL B. MILLER, et al., Unit Level Predicted Yield: a Method of Identifying High Defect Density Die at Wafer Sort, IEEE 2001, 1118-1127 | | | | |
| | | PHILIPPE LEJEUNE, et al., Optimizing Yield vs. DPPM for Parts Average Testing, www.galaxysemi.com | | | | |
| | | EMILIO MIGUELANEZ, et al., Advanced Automatic Parametric Outlier Detection Technologies for the Production Environment, | | | | |
| | | Guidelines for Part Average Testing, Automotive Electronics Council, AEC-Q001-Rev-C July 18, 2003 | | | | |
| | | ZINKE, KEVIN, et al. Yield Enhancement Techniques Using Neural Network Pattern Detection, IEEE 1997, 211-215 | | | | |
| | | LEJEUNE, PHILIPPE et al., Minimizing Yield Loss with Parts Average Testing (PAT) and Other DPM Reduction Techniques, Tetradyne Users Group, 2006 | | | | |
| | | LEJEUNE, PHILIPPE et al., Minimizing Yield Loss with Parts Average Testing (PAT) and Other DPM Reduction Techniques (PRESENTATION), Tetradyne Users Group, 2006 | | | | |
| | | | | | | |

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| Examiner Signature | Date Considered | |
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| Sheet | 5 | of | 5 | Attorney Docket Number | TAI.0800 |

| NON PATENT LITERATURE DOCUMENTS | | | | | | |
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| | | Defecter(tm)II - Defect Data Analysis Software, Semicon | | | | |
| | | STANLEY, JAMES, Spatial Outlier Methods for Detecting Defects in Semiconductor Devices at Electrical Probe, Motorola | | | | |
| | | RATCLIFFE, JEFF, Setting a Nearest Neighbor IDDQ Threshold, | | | | |
| | | DAASCH, ROBERT, Variance Reduction Using Wafer Patterns in Iddq Data, Proceeding of International Test Conference October 2000, pp 189-198 | | | | |
| | | DAASCH, ROBERT, Neighbor Selection for Variance Reduction in Iddq and Other Parametric Data, ITC International Test Conference, IEEE 2001 | | | | |
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